CLAIMS

What is claimed is:

1. An integrated detector circuit, comprising:

a first gain stage having an input that monitors a high frequency signal for routing a first detection current to a node; and

a second gain stage including a first current source for supplying a bias current indicative of a predefined amplitude of the high frequency signal, and having an input for monitoring the high frequency signal to route a portion of the bias current to the node as a second detection current, wherein the second detection current is limited to the bias current when the high frequency signal is greater than the predefined amplitude.

2. The integrated detector circuit of claim 1, wherein the second gain stage includes a first transistor having a control electrode coupled for receiving the high frequency signal and a first conduction electrode coupled to the node for supplying the second detection current.

3. The integrated detector circuit of claim 2, wherein the current source includes a second transistor having a conduction electrode coupled to a second conduction electrode of the first transistor.

4. The integrated detector circuit of claim 3, wherein the first transistor is an n-channel metal oxide semiconductor field effect transistor (MOSFET) having a gate that functions as the control electrode and the second transistor is a p-channel MOSFET having a drain that functions as the conduction electrode.

5. The integrated detector circuit of claim 2, further comprising a third gain stage having an input that monitors the high frequency signal for routing a third detection current to the node.

6. The integrated detector circuit of claim 5, wherein the first gain stage includes:

a second current source for supplying a second bias current; and

a second transistor having a control electrode coupled for receiving the high frequency signal and a first conduction electrode for routing a portion of the second bias current to the node as the second detection current.

7. The integrated detector circuit of claim 6, wherein the first and second transistors are scaled to a ratio and the first and second detection currents are scaled to the ratio when the high frequency signal is zero.

8. The integrated detector circuit of claim 1, further comprising an amplifier having a first input coupled to receive a reference signal, a second input coupled to the node, and an output for maintaining the node at a predetermined potential.

9. The integrated detector circuit of claim 1, wherein the high frequency signal operates at a frequency greater than four hundred megahertz.

10. A detector circuit, comprising gain stages that include current sources for establishing maximum current levels in the gain stages at corresponding amplitudes of a high frequency signal, wherein the gain stages function with transfer functions that convert the high frequency signal to detection currents for summing at a common node to produce an output detection signal as a substantially linear function of the high frequency signal, wherein the detection currents reach the maximum current levels at the corresponding amplitudes to compensate for nonlinearities in the transfer functions.

11. The detector circuit of claim 10, wherein the gain stages include transistors whose control electrodes are coupled to an input of the detector circuit and whose sources are coupled to the common node for providing the detection currents.

12. The detector circuit of claim 10, further comprising:

an amplifier having a first input for receiving a reference voltage and a second input coupled to the common node; and

a transistor having a control electrode coupled to an output of the amplifier and a conduction electrode coupled to the common node.

13. A method of detecting a high frequency signal, comprising the steps of:

amplifying a high frequency signal with a first transconductance to produce a first detection current;

amplifying the high frequency signal with a second transconductance to produce a second detection current for summing with the first detection current to produce an output signal; and

limiting the first detection current to a constant value to compensate for a nonlinearity in the second transconductance when the high frequency signal is greater than a predefined amplitude.

14. The method of claim 13, wherein the step of limiting includes the steps of:

generating a bias current with a current source; and

routing a portion of the bias current through a transistor with the high frequency signal to produce the first detection current.

15. The method of claim 13, further comprising the step of summing the first and second detection currents at a node to produce an output signal.

16. The method of claim 15, further comprising the steps of:

developing a reference voltage with a reference current; and

amplifying a difference between the reference voltage and a potential at the node to produce a correction signal that maintains the potential at the node substantially constant.

17. The method of claim 11, wherein the step of amplifying a high frequency signal with a first transconductance includes the step of converting a signal operating at a frequency greater than about four hundred megahertz to the first detection current.

18. A detector circuit, comprising:

a current source for providing a bias current;

a first transistor operating in response to a high frequency signal and having a first width and a first conduction electrode coupled to a node for producing a portion of the bias current as a first detection current; and

a second transistor operating in response to the high frequency signal, having a second width less than the first width, and having a first conduction electrode coupled to the node for producing a second detection current for summing with the first detection current to produce an output signal.

19. The detector circuit of claim 18, wherein the first detection current has a value substantially equal to the bias current when the high frequency signal is greater than a predefined amplitude to compensate for a nonlinearity in a transfer function of the second transistor.

20. The detector circuit of claim 19, further comprising a third transistor having a conduction electrode coupled to a second conduction electrode of the first transistor to supply the bias current.